## ABSTRACT

According to one embodiment, a memory cell structure comprises a semiconductor substrate, a first silicon oxide layer situated over the semiconductor substrate, a charge storing layer situated over the first silicon oxide layer, a second silicon oxide layer situated over the charge storing layer, and a gate layer situated over the second silicon oxide layer. In the exemplary embodiment, the charge storing layer comprises silicon nitride having reduced hydrogen content, e.g., in the range of about 0 to 0.5 atomic percent. As a result, the reduced hydrogen content reduces the charge loss in the charge storing layer. The reduced charge loss in the charge storing layer has the benefit of reducing threshold voltage shifts, programming data loss, and programming capability loss in the memory device, thereby improving memory device performance.

**Figure 2 should accompany the Abstract.**